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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Philippe Diehl

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EXAMINER

CHRISS, ANDREW W

ART UNIT

PAPER NUMBER

2472

MAIL DATE

DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/673,665	Applicant(s) DIEHL ET AL.	
	Examiner ANDREW CHRISS	Art Unit 2472	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 9-14, 20-24 and 28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 9-14, 20-24, and 28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Applicant's amendment, filed July 1, 2009, has been entered and carefully considered. Claims 5-8, 15-19, and 25-27 are canceled, and Claims 1-4, 9-14, 20-24, and 28 are currently pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claim 28** is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for multiple signal inclusion schedules, does not reasonably provide enablement for one signal inclusion schedule being different than another. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Applicant's specification discloses, at paragraph 61, send and receive portions sharing a common storage unit for storing their respective schedules. However, the cited portion of Applicant's specification does not provide either explicit or implicit support for the schedules being different than one another or any characteristic that would distinguish one schedule from another.

4. **Claim 28** rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the

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inventors, at the time the application was filed, had possession of the claimed invention.

Applicant's specification, as originally filed, does not disclose a first and second signal inclusion schedule being different from one another. Therefore, the claim limitation "wherein the first signal inclusion schedule and the second signal inclusion schedule are different signal inclusion schedules" constitutes new matter.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 1-3, 9-13, and 20-24** rejected under 35 U.S.C. 103(a) as being unpatentable over Reblewski et al (United States Patent 6,265,894), hereinafter Reblewski, in view of Kappler et al (United States Patent 6,064,677), hereinafter Kappler, and Duan et al (United States Patent 5,923,656), hereinafter Duan.

Regarding Claims 1 and 9, Reblewski teaches a reconfigurable integrated circuit for use in an emulation system (column 1, line 66 – column 2, line 2). However, Reblewski does not teach a storage unit comprising a signal inclusion schedule or circuitry operative to generate and transmit a message. In the same field of endeavor, Kappler teaches a calendar queue mechanism for scheduling transport of units or cells, specifically high frequency/high priority flows and low frequency/low priority flows (column 12, line 65 – column 13, line 10). Further, Kappler teaches a set of transmit lists 65, connected to calendar queue 63 (Figure 3), which generate and transmit the messages released by the calendar queue (column 11, lines 25-30). As mentioned above, the calendar queue specifies the frequency of the signals to include. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms. However, the aforementioned references do not disclose selecting a plurality of signals from at least one pin. In the same field of endeavor, Duan discloses a cell scheduler in an ATM switch fabric that selects a “winning” set of cells (i.e., plurality of signals) from multiple FIFO rooms in a memory (Figure 2; column 7, lines 17-35 and 53-64). Although Duan does not explicitly disclose selecting the signal from a pin, Examiner takes Official Notice that implementation of ATM switch fabrics in integrated circuits is well-known in the art, and therefore it would have been obvious to one of ordinary skill in the art that the selection of a cell for transfer would comprise transmission over an IC pin. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the scheduler disclosed in Duan with the reconfigurable integrated disclosed in

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Reblewski, as modified above, in order to maximize transmission opportunities for available ports in an ATM switch fabric (see column 3, lines 18-29 of Duan).

Regarding Claims 2 and 10, Reblewski does not teach signals determined to be more critical transmitted more frequently. In the same field of endeavor, Kappler further teaches flows having different frequencies are prioritized so that the data transport units of the higher frequency flows are given transmit priority over any data transport units of lower frequency flows with which they happen to collide (column 12, lines 30-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 3 and 12, Reblewski does not teach generating and transmitting a message in a plurality of clock cycles of an operating clock independent of an emulation clock. In the same field of endeavor, Kappler further teaches that the calendar queue 63 implements a stalled virtual clock so that cells that are scheduled for transmission are leased for transmission only when system “real time” has reached their respective scheduled transmission times (column 11, lines 21-25). Therefore, messages are generated in a plurality of clock cycles of an operating clock independent of the predetermined rate of the overall system clock (column 8, lines 53-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to reduce relative data

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transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 11, Reblewski does not teach the message comprising state values. In the same field of endeavor, Kappler teaches that each outbound message contain VP and VC identifiers (Figure 2), equivalent to Applicant's disclosed state value (Figure 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 13, Reblewski does not teach extracting a parity value from a message. In the same field of endeavor, Kappler teaches reading a CRC (parity) value from an inbound cell (Figure 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 20, Reblewski teaches an integrated circuit for use in an emulation system, as described with regards to Claims 1 and 9. Reblewski further teaches multiple reconfigurable logic resources (Figure 2), output pins 113, and a partial scan register that receives a plurality of output signals from logic elements (column lines 6-15), equivalent to Applicant's claimed message formation and send block. However, Reblewski does not teach a signal inclusion schedule. In the same field of endeavor, Kappler teaches a signal inclusion

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schedule, as discussed with regards to Claims 1 and 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms. However, the aforementioned references do not disclose selecting a plurality of signals from at least one pin. In the same field of endeavor, Duan discloses a cell scheduler in an ATM switch fabric that selects a “winning” set of cells (i.e., plurality of signals) from multiple FIFO rooms in a memory (Figure 2; column 7, lines 17-35 and 53-64). Although Duan does not explicitly disclose selecting the signal from a pin, Examiner takes Official Notice that implementation of ATM switch fabrics in integrated circuits is well-known in the art, and therefore it would have been obvious to one of ordinary skill in the art that the selection of a cell for transfer would comprise transmission over an IC pin. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the scheduler disclosed in Duan with the reconfigurable integrated disclosed in Reblewski, as modified above, in order to maximize transmission opportunities for available ports in an ATM switch fabric (see column 3, lines 18-29 of Duan).

Regarding Claim 21, Reblewski teaches an input pin 113. Reblewski further teaches a logic element that receives multiple inputs and outputs a single signal (truth table 202). However, Reblewski does not teach the claimed message receive and disassembly block nor the signal inclusion schedule. In the same field of endeavor, Kappler teaches a switching fabric that decomposes cells into four bit wide “nibbles” for arbitration and routing (column 10, lines 7-13), equivalent to Applicant’s claimed message received and disassembly block. Kappler further

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teaches a signal inclusion schedule, as discussed with regards to Claims 1 and 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 22, Reblewski teaches a plurality of output pins 113. Further, Reblewski teaches an array of reconfigurable integrated circuits in Figure 10, thereby teaching multiple partial scan registers.

Regarding Claim 23, Reblewski teaches an array of reconfigurable integrated circuits in Figure 10, thereby teaching a plurality of reconfigurable logic resources in communication with the message formation and send block.

Regarding Claim 24, Reblewski teaches an integrated circuit for use in an emulation system, as described with regards to Claims 1, 9, and 20. Reblewski further teaches multiple reconfigurable logic resources (Figure 2) and input pins 113. However, Reblewski does not teach the claimed message receive and disassembly block nor the signal inclusion schedule. In the same field of endeavor, Kappler teaches a switching fabric that decomposes cells into four bit wide “nibbles” for arbitration and routing (column 10, lines 7-13), equivalent to Applicant’s claimed message received and disassembly block. Kappler further teaches a signal inclusion schedule, as discussed with regards to Claims 1 and 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed

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outputs from output queued routing mechanisms. However, the aforementioned references do not disclose selecting a plurality of signals from at least one pin. In the same field of endeavor, Duan discloses a cell scheduler in an ATM switch fabric that selects a “winning” set of cells (i.e., plurality of signals) from multiple FIFO rooms in a memory (Figure 2; column 7, lines 17-35 and 53-64). Although Duan does not explicitly disclose selecting the signal from a pin, Examiner takes Official Notice that implementation of ATM switch fabrics in integrated circuits is well-known in the art, and therefore it would have been obvious to one of ordinary skill in the art that the selection of a cell for transfer would comprise transmission over an IC pin. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the scheduler disclosed in Duan with the reconfigurable integrated disclosed in Reblewski, as modified above, in order to maximize transmission opportunities for available ports in an ATM switch fabric (see column 3, lines 18-29 of Duan).

8. **Claims 4 and 14** rejected under 35 U.S.C. 103(a) as being unpatentable over Reblewski in view of Kappler and Duan as applied to claims 1 and 13 above, and further in view of Sindhushayana et al (United States Patent Application Publication US 2003/0053435 A1), hereinafter Sindhushayana. Reblewski, Kappler, and Duan teach all of the limitations of Claims 1 and 13, as discussed above. However, the references do not teach a parity bit generator. In the same field of endeavor, Sindhushayana teaches a channel interleaver that permutes systematic bits with parity bits, thus generating a parity value and transmitting a message containing a parity value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the parity value generator taught in Sindhushayana with the reconfigurable

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emulation integrated circuit taught in Reblewski, as modified above, in order to employ an error correction system that overcomes the impact of interference in a wireless system.

9. **Claim 28** rejected under 35 U.S.C. 103(a) as being unpatentable over Reblewski in view of Kappler and Duan as applied to Claim 24 above, and further in view of Parruck et al (United States Patent 6,198,723), hereinafter Parruck. The combination of Reblewski, Kappler, and Duan discloses all of the limitations of Claim 24, as described above. However, the aforementioned references do not disclose different signal inclusion schedules. In the same field of endeavor, Parruck discloses a traffic shaping device using multiple round robin schedulers (Figure 4, 212; column 7, lines 61-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multiple schedulers disclosed in Parruck with the reconfigurable IC disclosed in Reblewski, as modified above, in order to shape output traffic and meet quality of service criteria.

Response to Arguments

10. Applicant's arguments, filed July 1, 2009, with respect to rejection of Claims 21, 24, and 28 under 35 U.S.C. 112, first paragraph, for failing to comply with the enablement requirement have been fully considered and are persuasive. The rejection of Claims 21, 24, and 28 under 35 U.S.C. 112, first paragraph, for failing to comply with the enablement requirement has been withdrawn.

11. Applicant's arguments filed July 1, 2009 regarding rejection of Claim 28 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement have been fully considered but they are not persuasive. Applicant's specification discloses, at paragraph 61,

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send and receive portions sharing a common storage unit for storing their respective schedules. However, the cited portion of Applicant's specification does not provide either explicit or implicit support for the schedules being different than one another or any characteristic that would distinguish one schedule from another. Therefore, the claim limitation "wherein the first signal inclusion schedule and the second signal inclusion schedule are different signal inclusion schedules" is not supported and therefore constitutes new matter. Rejection of Claim 28 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

12. Applicant's arguments, filed July 1, 2009, with respect to the rejection of claims 1-4, 9-14, 20-24, and 28 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of ATM switch fabric performing cell scheduling and cell output disclosed in Duan.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDREW CHRISS whose telephone number is (571)272-1774. The examiner can normally be reached on Monday - Friday, 7:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on 571-272-7872. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew Chriss
Examiner
Art Unit 2472
11/1/2009

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